REQUEST FOR RECONSIDERATION
AFTER FINAL
August 16, 2006

YOR920030249US1
Serial No. 10/644,210

REMARKS

Claims 1 – 29 remain in the application and are finally rejected under 35 U.S.C. §102(e) over published U.S. Patent Application No. 2004/0010675 to Moritz. The final rejection is respectfully traversed.

In responding to the applicants' remarks with the previously filed amendment, the final Office action asserts that "[a]s to the storage arrays not being buffered, before or after the array, the cache array is the buffer. Applicant appears to be misusing this terminology. The claim language does not require a separate buffer from the cache itself." Claim 1, for example recites a "cache memory" that includes "a cache **buffer** containing most recently accessed data;" and "a storage array ... selectively receiving data from said cache buffer," and selectively storing data from the cache buffer. Lines 1 – 5. Thus, very clearly the claims recite a buffer (cache buffer) for the cache array (the storage array) and applicants are not misusing the terminology. Further, if "the cache array is the buffer," how does the cache array selectively receive data from itself? In other words, if "the cache array is the buffer," how is the "storage array (i.e., the cache array) ... selectively receiving data from said cache buffer (i.e., the cache array)," and does it selectively store data from itself? Unless data in the cache array can somehow be shown to be segregated, which it is not in any reference of record, interpreting the "the cache array [to be] the buffer," renders the claims nonsensical. "During patent examination, the pending claims must be 'given *>their< broadest **reasonable** interpretation **consistent with the specification**.' >*In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). MPEP §2111 (emphasis added).

The final Office action further responds that "[a]s to the storage arrays not communicating with one another, this is not a claim limitation." For the "storage array ... [to] selectively [receive] data from said cache buffer," there must be communication between the two. Without communication between the storage array and the cache buffer, one cannot receive anything from the other and vice versa. Further, as provided in

claims 3 – 8, 11 – 18 and 19 – 29, the cache buffer may specifically include an input buffer and an output buffer, each buffering the storage array. An input buffer that has no communications path with what it is buffering is not a buffer. Thus, the claims clearly reflect elements communicating with one another; and, "a storage array ... selectively receiving data from said cache buffer," is neither shown, nor suggested, by any reference of record.

Furthermore, in finally rejecting the present application it is again asserted that claim 1 (and claim 10 and claim 19) is taught by Moritz Figure 4 and paragraphs 0105 – 0109. Specifically regarding how the claims are read on Moritz Figure 4, it is asserted that "a cache buffer containing most recently accessed data as a multi-bank structure as a cache memory having multiple ways with the ways being equivalent to banks with Tag-Cache being a buffer structure which stores cache line **addresses** for the most recently accessed cache lines (e.g., see Figure 4, element 210 and paragraph 0105);" (emphasis added). The discussion of element 210 in paragraph 0105 is directed to avoiding resorting to a "conventional associative lookup mechanism" for determining a cache line address. While Moritz certainly teaches the Tag-Cache 210 storing cache line addresses in paragraphs 0116 – 118, that is not what claim 1 recites, at least for the cache buffer. As noted hereinabove, the cache buffer contains "most recently accessed data;" not "cache line **addresses** for the most recently accessed cache lines" as has been asserted. At the end of paragraph 0118, Moritz also indicates that "each Tag-Cache 210 entry is exactly the same as a hotline register 208, and performs the same functions, but dynamically." So, a Moritz Tag-Cache 210 like the

> hotline register 208 has 3 components: (1) protection bits (ASID), which are used to enforce address space protection, (2) TagIndex--two accesses are to the same cache line if their Tag and Index components are the same. The TagIndex component is compared with Tag and Index of the actual access to check if the hotline register can indeed be used to directly address the cache, (3) cache-way information—this information enables direct access to one of the ways in the set-associative cache.

Paragraph 0115. Therefore, while both the Tag-Cache 210 and the hotline register 208 store cache line addresses for data in the Moritz data arrays, neither stores "most recently accessed data;" as recited in the finally rejected claims.

Further claim 1, for example, also recites "a tag memory storing tags associated with data in said storage array and selected data in said cache buffer." Lines 6 – 7. Even if one were to accept *arguendo*, that the Moritz Tag-Cache 210 were a cache buffer within a reasonable interpretation of the present specification, there is nothing in either the Moritz Tag-Cache 210 or the Moritz hotline register 208 that could be considered as "storing tags associated with ... selected data in" the Moritz Tag-Cache 210. Certainly, the Moritz "Hotline MISS" line is not a tag "associated with ... selected data in said cache buffer." *Id.*

Therefore, Moritz fails to teach a cache buffer that contains "most recently accessed data," as recited by claims 1 and 10, and fails to teach "selectively loading accessed data from said storage array to an output buffer, a number of most recently accessed data blocks being held in said output buffer" as claim 19 recites. Therefore, Moritz does not teach the present invention as recited in claims 1, 10 or 19.

Furthermore, because dependent claims include all of the differences with the cited reference as the claims from which they depend, claims 2 – 8, 11 – 18 and 20 – 29, are neither taught, nor suggested by Moritz, alone or, further in combination with any reference of record. Reconsideration and withdrawal of the final rejection to claims 1 – 29 under 35 U.S.C. §102(e) over Moritz is respectfully requested.

The applicant thanks the Examiner for efforts, both past and present, in examining the application. Believing the application to be in condition for allowance for the reasons set forth above, the applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 1 – 29 under 35 U.S.C. §102(e) and allow the application to issue.

REQUEST FOR RECONSIDERATION
AFTER FINAL
August 16, 2006

YOR920030249US1
Serial No. 10/644,210

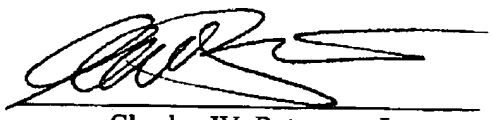
The applicant notes that MPEP §706 "Rejection of Claims," subsection III, "PATENTABLE SUBJECT MATTER DISCLOSED BUT NOT CLAIMED" provides in pertinent part that

> If **the examiner** is satisfied after the search has been completed that patentable subject matter has been disclosed and the record indicates that the applicant intends to claim such subject matter, he or she **may note** in the Office action that **certain aspects or features** of the patentable invention have not been claimed and that if properly claimed such claims **may be given favorable consideration.**

(emphasis added.) The applicant believes that the matter presented in the written description of the present application is quite different than, and not suggested by, any reference of record. Accordingly, should the Examiner believe anything further may be required, the Examiner is requested to contact the undersigned attorney at the local telephone number listed below for a telephonic or personal interview to discuss any other changes.

Please charge any deficiencies in fees and credit any overpayment of fees to IBM Corporation Deposit Account No. 50-0510 and advise us accordingly.

Respectfully Submitted,



August 16, 2006
(Date)

Charles W. Peterson, Jr.
Registration No. 34,406

Customer No. 33233
Law Office of Charles W. Peterson, Jr.
Suite 100
11703 Bowman Green Drive
Reston, Virginia
Telephone: (703) 481-0532
Facsimile: (703) 659-1485